TUNDRA

Universe II Specific Register

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Universe II Specific Register

INTRODUCTION

This document describes the operation of the Universe II's "Specific Register" (U2SPEC, offset 0x4FC). This register can be used to improve the performance of the Universe II by reducing the latency of key VMEbus timing elements. This register is present in versions of the Universe device that have a Revision ID of 01 (defined in the PCI_CLASS register, offset 008).
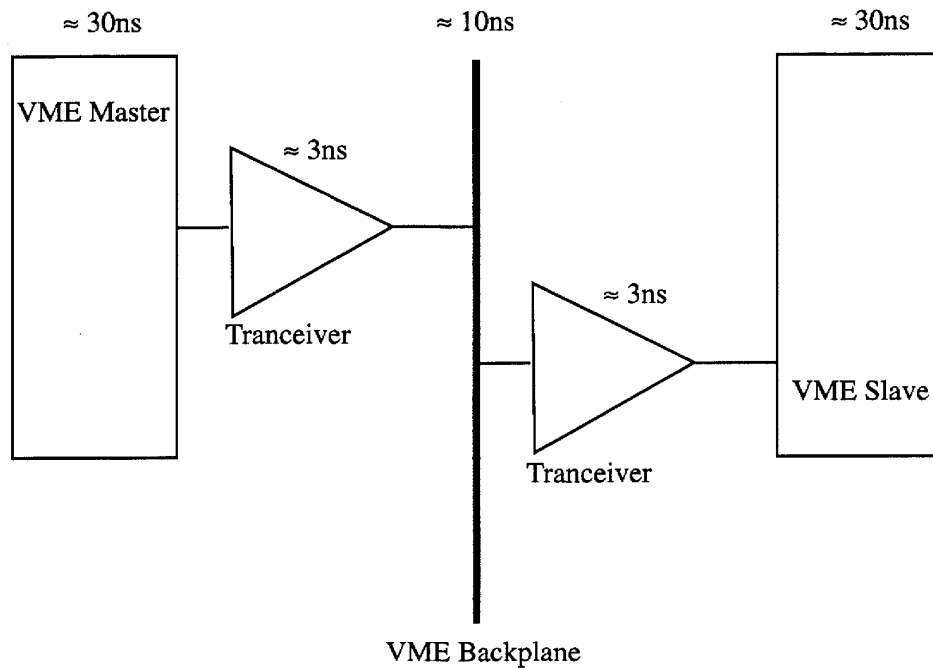
⚠ *The U2SPEC register is an unsupported feature of Universe II. Its design may not be as robust as other areas of the Universe II design, and may not be included in future revisions of the device. Improper use of the U2SPEC Register may result in undesirable system behaviour. Tundra Semiconductor Corporation does not recommend the manipulation of this register by users who are unfamiliar with the timing characteristics of their VME systems.*

OVERVIEW OF THE U2SPEC REGISTER

Although the VMEbus is asynchronous, there are a number of maximum and minimum timing parameters that must be adhered to (as detailed in the *VME64 Specification*). In order to qualify as compliant, master, slave and location monitor devices must guarantee that they meet these timing parameters *independent of their surroundings*. That is to say, they must assume zero latency between themselves and the VMEbus. This is, however, never the case. Buffers, transceivers and the backplane itself, all introduce latencies that combine to produce additional system delay (see Figure 1). The consequence of such delay is the degradation of overall performance.

The Universe II's U2SPEC Register allows users to compensate for the latencies that are inherent in their VMEbus system designs. Through the use of this register, users can reduce the inherent delay associated with five key VMEbus timing parameters. Using the U2SPEC register may result in violation of the VME specification.

$\approx$ 30ns $\approx$ 10ns $\approx$ 30ns

```
┌──────────┐                    │                    ┌──────────┐
│VME Master│      ≈ 3ns         │                    │          │
│          │    ◁────           │                    │          │
│          │   Tranceiver       │     ≈ 3ns          │          │
│          │                    │    ◁────           │VME Slave │
│          │                    │   Tranceiver       │          │
│          │                    │                    │          │
└──────────┘                    │                    └──────────┘
```

VME Backplane

Note: All times are approximate and
         are used for illustration purposes
         only.

Figure 1:   Sources of VME System Latency

ADJUSTABLE VME TIMING PARAMETERS

VME DTACK* Inactive Filter (DTKFLTR)

In order to overcome the DTACK* noise typical of most VME systems, the Universe II quadruple samples this signal with the 64MHz clock. While "safer", the extra sampling results in decreased performance. Users who believe their systems to have little noise on their DTACK* lines can elect to filter this signal less and thus increase their Universe II response time.

VME Master Parameter t11 Control (MASt11)

According to the VME64 Specification, a VMEbus master must not drive DS0* low until both it and DS1* have been simultaneously high for a minimum of 40ns. The MASt11 parameter in the U2SPEC Register, however, allows DS0* to be driven low in less than 40ns.

VME Master Parameter t27 Control (READt27)

During read cycles, the VMEbus master must guarantee that the data lines will be valid within 25ns after DTACK* is asserted. That is to say, the master must not latch the data and terminate the cycle for a minimum of 25ns after the falling edge of DTACK*. The READt27 parameter in the U2SPEC register allows for faster cycle termination in one of two ways. One setting allow for the data to be latched and the cycle terminated with an associated delay that is less than 25ns. The second results in no delay what-so-ever in latching and termination.

VME Slave Parameter t28 Control (POSt28)

According the *VME64 Specification*, VMEbus slaves must wait at least 30ns after the assertion of DS* before driving DTACK* low. The POSt28 parameter in the U2SPEC Register, however, allows DTACK* to be asserted in less than 30ns when executing posted writes.

VME Slave Parameter t28 Control (PREt28)

VMEbus slaves must wait at least 30ns after the assertion of DS* before driving DTACK* low. The PREt28 parameter in the U2SPEC Register, however, allows DTACK* to be asserted in less than 30ns when executing prefetched reads.

Table 1 - Universe II Specific Register (U2SPEC)

Register Name: U2SPEC						Offset: 4FC	

Bits	Function						
31-24	Universe Reserved						
23-16	Universe Reserved						
15-08	Universe Reserved		DTKFLTR	Reserved	MASt11	READt27	
07-00	Universe Reserved				POSt28	Reserved	PREt28

U2SPEC Description

Name	Type	Reset By	Reset State	Function
DTKFLTR	R/W	all	0	VME DTACK* Inactive Filter 0=Slower but better filter, 1=Faster but poorer filter
MASt11	R/W	all	0	VME Master Parameter t11 Control (DS* high time during BLT's and MBLT's) 0=Default, 1=Faster
READt27	R/W	all	00	VME Master Parameter t27 Control (Delay of DS* negation after read) 00=Default, 01=Faster, 10=No Delay
POSt28	R/W	all	0	VME Slave Parameter t28 Control (Time of DS* to DTACK* for posted-write) 0=Default, 1=Faster
PREt28	R/W	all	0	VME Slave Parameter t28 Control (Time of DS* to DTACK* for prefetch read) 0=Default, 1=Faster

For a detailed explanation of the above options, please see the section "Adjustable VME Timing Parameters", above.